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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	3638US (98-0093)
First Inventor or Application Identifier	Salman Akram et al.
Title	HIGH DENSITY MODULARITY FOR IC'S
Express Mail Label No.	EL248225241US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

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1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original, and a duplicate for fee processing)*
2. [X] Specification [Total Pages 21] *(preferred arrangement set forth below)*
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [Total Sheets 11]
4. Oath or Declaration [Total Pages 1]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F R. § 1 63(d)) *(for continuation/divisional with Box 17 completed)* ***[Note Box 5 below]***
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6. [ ] Microfiche Computer Program *(Appendix)*
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ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [X] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [X] Information Disclosure Statement (IDS)/PTO-1449 [X] Copies of IDS Citations
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APPLICATION FOR LETTERS PATENT

for

HIGH DENSITY MODULARITY FOR IC'S

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HIGH DENSITY MODULARITY FOR IC'S

BACKGROUND OF THE INVENTION

Field of the Invention: This invention relates generally to integrated circuit (IC) or semiconductor devices. More particularly, the invention pertains to integrated circuit configurations which provide high density modules for mounting on circuit boards and other host apparatus.

State of the Art: Integrated circuit semiconductor devices (IC's) are small electronic circuits formed on the surface of a wafer of semiconductor material such as silicon. The IC's are fabricated in plurality as part of a wafer. The wafer is then subdivided into discrete IC chips or dice, and then further tested and assembled for customer use through various well-known individual die testing and packaging techniques, including lead frame packaging, Chip-On-Board (COB) packaging, and flip-chip packaging (FCP). Depending upon the die and wafer sizes, each wafer is divided into a few dice or as many as several hundred or more than one thousand discrete dice, each of which becomes an IC package.

The continuing demand for miniaturization has resulted in the development of integrated circuits on dice of very small size. The corresponding miniaturization of external circuitry has not proceeded at the same rate. Thus, there is a need for devices (including the interconnecting circuitry) of increasingly greater density.

Multi-chip modules have typically followed the convention of earlier, single chip packages, in that the reverse sides of bare dice or chips are mounted on a substrate such as a printed circuit board (PCB), leaving the active surface exposed for wire-bonding to the substrate or leadframe. Such is exemplified in United States Patent 4,873,615 of Grabbe. Typically, dice are attached to one side only of the substrate, as in United States Patents 4,992,849 and 4,992,850 of Corbett et al.

Where the device encompasses dice on both sides of the substrate, the reverse sides of the dice are conventionally attached to the substrate, as illustrated in United States Patent 5,239,198 of Lin et al.

Stacked groups of packaged devices, often called cubes, have been developed, as exemplified in United States Patent 5,016,138 of Woodman, United States Patent 5,128,831 of Fox, III et al., United States Patent 5,291,061 of Ball, United States Patent 5,420,751 of Burns, United States Patent 5,455,445 of Kurtz et al., United States Patent 5,602,420 of Ogata et al., and United States Patent 5,637,912 of Cockerill et al. In these references, each non-conductive substrate has one or more IC dies attached to one side only, or where dies are attached to both sides of the substrate, not more than one die is so attached on its active surface. In variants where there is no existing substrate between adjacent dice or packages, the packages have peripheral external leads

In United States Patent 5,291,061 of Ball and United States Patent 5,323,060 of Fogal et al., multiple dice are stacked and wire-bonded to circuitry on a substrate with progressively longer wires.

Dice having areal bond pads, i.e. on the active surface, complicate the construction of multi-chip modules, particularly when wire-bonding is the connection method of choice. As taught in United States Patent 5,012,323 of Farnworth, United States Patents 5,422,435, 5,495,398 and 5,502,289 of Takiar et al., and United States Patent 5,600,183 of Gates, Jr., bonding with wire or other conductor necessitates that the stacked dice be of progressively smaller size.

In United States Patent 4,996,587 of Hinrichsmeyer et al. and United States Patent 5,107,328 of Kinsman, a package is shown with a die within a recess in a carrier. The carrier has shelves which extend over the die, leaving a slot through which the die is wire-bonded to conductive traces on the opposite surface of the shelves. United States Patent 5,677,569 of Choi et al. shows a stacked package in which holes in the substrate permit wire-bonding of die pads to the upper surface of the substrate.

In United States Patent 5,438,224 of Papageorge et al. and United States Patent 5,477,082 of Buckley, III et al, a pair of dice are shown attached on their active surfaces to opposite sides of an intermediate layer such as a substrate. In both references, the terminals on the dice are directly coupled to terminals on the same side of the

intermediate member by e.g. solder balls. The opposed dice are shown as being coextensive.

BRIEF SUMMARY OF THE INVENTION

In one aspect, the invention comprises a method for forming a high density multi-chip module (MCM) from a plurality of integrated circuits (IC's) in the form of bare dice with one or more rows of conductive bond pads. The bond pads of each die are preferably formed in a row or rows generally spanning the active surface. The dice are mounted on opposing sides of a substrate in a staggered flip-chip style and wire-bonded through-slots to conductors on the opposite side of the substrate. Metallization in the form of conductive leads on both surfaces of the substrate are thus connected by wire bonds to the dice, and to an electrical Input/Output (I/O) means such as a ball-grid array (BGA), edge connector, etc. for connection to an external circuit.

In another aspect, the invention comprises the multi-chip module formed by the method.

In one preferred form, an array of solder balls is formed on one surface of the substrate, in the peripheral area surrounding the die or dice mounted on that surface. Alternatively, a pin-grid array may be used. The multi-chip module may be readily attached by surface mounting on a circuit board for example.

In another preferred form, an edge connector such as a socket connector as well-known in the art may be used.

The bonded wires within the through-slots in the substrate are preferably surrounded with a "glob-top" sealant material following testing. Thus, the wire connections are sealed by glob-top on one side of the substrate, and by the die bonding material on the opposite side of the substrate. A minimum amount of glob-top material is required.

The module construction permits testing of each die after wire-bonding, and easy removal and replacement of a defective die, if necessary, without removal of any encapsulant material. The construction is such that the bonded conductive wires are,

prior to glob top application, protected from physical damage by their location within through-slots in the substrate, and between or adjacent opposing dies. The opportunity for damage during die testing or die replacement prior to wire encapsulation is greatly reduced.

The module of the invention has a high density, inasmuch as it is formed as an array of bare dice rather than encapsulated packages of greater size. Dice are mounted on both sides of a substrate to form the module, and coplanar dies may be closely spaced, leaving room enough for forming the wire-bonds within the through-slots.

The method of the invention may be employed to surface mount bare dice on e.g. a printed circuit board of an electronic component.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention is illustrated in the following exemplary figures, wherein the drawings are not necessarily to scale.

FIG. 1 is a perspective upper view of a high density IC module of the invention;

FIG. 2 is a perspective lower view of a high density IC module of the invention;

FIG. 3 is a top view of a high density IC module of the invention, in an intermediate stage of fabrication;

FIG. 4 is a bottom view of a high density IC module of the invention, in an intermediate stage of fabrication;

FIG. 5 is a cross-sectional edge view of a high density IC module of the invention, as taken along line 5-5 of FIG. 1;

FIG. 6 is a cross-sectional edge view of a high density IC module of the invention, as taken along line 6-6 of FIG. 5;

FIG. 7 is a partial cross-sectional view of another embodiment of a high density IC module of the invention;

FIG. 8 is a partial cross-sectional view of another embodiment of a high density IC module of the invention;

FIG. 9 is a top view of a high density IC module of the invention, in an intermediate stage of fabrication;

FIG. 10 is a bottom view of a high density IC module of the invention, in an intermediate stage of fabrication; and

FIG. 11 is a perspective top view of another embodiment of a high density IC module of the invention.

DESCRIPTION OF THE ILLUSTRATED EMBODIMENTS

An exemplary embodiment of the invention is illustrated in drawing FIGS. 1 through 8 and is shown as a high density module 10 having two IC dies 12A, 12B mounted on a first side 16 of a substrate 20. One IC die 14A is shown on the opposite (second) side 18 of the substrate, in a staggered position relative to dies 12A, 12B. While the figures show a total of three dies 12A, 12B, 14A in the module, any number may be mounted to substrate 20 to form a dense IC module for use as a memory device, for example. In a spacially balanced module, the numbers of dice on the first and second sides 16, 18 will differ by one.

The dice 12, 14 are attached to the substrate 20 by an adhesive layer 38, which may be any non-conductive adhesive or adhesive tape as known in the art.

Each of the IC dies 12A, 12B and 14A is a bare (unpackaged) die with one or more adjacent rows of bond pads 22 on an active side 24. In drawing FIGS. 1 and 2, the bond pads 22 of dies on the opposite side are not visible, being covered by a glob-top 40. In drawing FIGS. 5 to 8, two rows of bond pads 22 are shown spanning the minor dimension 26 of the dies (See FIG. 1). Alternatively, the bond pads 22 may be configured in a row or rows anywhere on the active surface 24, but preferably along a centerline 42 of a major dimension 28 or minor dimension 26, or even at an oblique angle with the major dimension. Preferably, the dice 12, 14 should be aligned so that the rows of bond pads 22 are in a parallel, spaced apart relationship.

The substrate 20 is shown with elongate through-slots 30A and 30B, each through-slot passing through the substrate between the first side 16 and the second side

18. The through-slots 30A, 30B are configured to provide access from the opposite side 18 of the substrate 20 for wire-bonding the bond pads 22 to connection sites 32 of a conductor pattern 34 on the substrate. The dice 12A and 12B are spaced a distance 36 apart, leaving room for the through-slot 30C therebetween.

As shown in drawing FIGS. 2 and 4 through 8, die 14A is mounted on the opposite side 18 of the substrate 20 between through-slots 30A and 30B. Like dice 12A and 12B, die 14A has its active surface 24 bonded to the substrate 20. Through-slot 30C encompasses the bond pads 22 of die 14A and is configured to provide access to the bond pads from the first side 16 of the substrate 20, i.e. from the side opposite the side to which the die 14A is attached.

Conductor patterns 34A, 34B are incorporated on each side 16, 18, respectively, of the substrate 20, having connection sites 32 adjacent each through-slot 30 for wire-bonding to bond pads 22 with conductive wires 44. The conductor patterns 34A, 34B and connection sites 32 are not shown in drawing FIGS. 1 through 4 for the sake of clarity, but are depicted in drawing FIGS. 5 through 8.

An exemplary conductor pattern 34A is shown on first substrate side 16 in drawing FIG. 9. The conductor pattern 34A has connection sites 32A for wire-bonding to die 14A (not shown in FIGS. 9 and 10) through through-slot 30C. In the example shown, the conductors 35A of conductor pattern 34A are also connected to solder balls 50 on side 18 (See FIG. 2) which comprise input/output connections for connecting the dice 12, 14 to external circuitry. The solder balls 50 comprise a ball-grid-array in a peripheral area 46 surrounding the die or dice. The balls are configured to be surface mounted to conductive traces on a larger substrate such as a circuit board, not shown. The input/output connections may also comprise a pin-grid-array (PGA), such an array well known in the art.

The conductor pattern 34A on side 16 of the substrate 20 is interconnected with the solder balls 40 or with conductor pattern 34B on side 18 by conductive vias 48 passing through the substrate.

The conductor pattern 34B has connection sites 32B for wire-bonding to dice 12A and 12B (not shown in FIGS. 9 and 10)) through through-slots 30A and 30B, respectively. In the example shown, the conductors 35B of conductor pattern 34B have outer ends 52B which are connected to solder balls 50 on the same side 18 (See FIG. 2).

As shown in drawing FIGS. 1 through 10, the module 10 has a separate solder ball 50 conductively connected to each bond pad 22 of the three dice 12A, 12B, 14A. Where the dice are to have common conductors, the number of solder balls 50 or other input/output connection lines will be much decreased.

A socket type connector 54 may be used instead of the ball-grid-array of balls 50, or pin-grid-array. As shown in drawing FIG. 11, a socket type connector 54 may be provided which permits vertical placement of the module on a circuit board, or cable connection. The conductor patterns 34A, 34B will vary from those of drawing FIGS. 9 and 10 in that the conductors 35A and 35B will extend to the socket type connector 54 rather than to an array of solder balls 50. Methods for making such patterns and connections are well known in the art.

Turning now specifically to drawing FIGS. 5 through 8, several variations in the through-slot configuration are illustrated.

A simple through-slot configuration in drawing FIGS. 5 and 6 has flat walls 56. The walls 56 are shown as parallel, but in an alternative arrangement, they may be beveled relative to each other. The through-slots 30A, 30B and 30C are shown with wires 44 bonded to bond pads 22 and connection sites 32A, 32B on substrate sides 16 and 18, respectively. The slot width 62 is such that it exposes the bond pads 22 and permits entrance of a wire bonding machine head for bonding the conductive wires 44. The slot length 60 exceeds the length of the row of bond pads 22, providing space for performing the wire-bonding.

Drawing FIGS. 7 and 8 correspond generally to drawing FIG. 5, but show different through-slot configurations, and do not show the glob-top 40. As depicted in drawing FIG. 7, through-slot 30C is formed with outwardly extending stepped surfaces 58 in opposed walls 56. These stepped surfaces 58 face the opposite side 16 of the substrate

20, and connection sites 32A on the stepped surfaces 58 are wire-bonded to bond pads 22 on die 14A with wires 44. In this configuration, stepped surfaces 58 are only slightly recessed from the substrate side 16.

In drawing FIG. 8, each through-slot step 58 is positioned much deeper in the substrate 20, shortening the length of the wires 44.

In drawing FIGS. 7 and 8, the wires 44 are effectively buried within the substrate 20, making them less prone to physical damage during handling of the module.

The method of making the module 10 of the invention comprises the following steps:

A plurality of integrated circuit dice 12, 14 are procured or fabricated. The integrated circuit dice 12, 14 are formed with an active surface 24 with one or more rows of conductive bond pads 22 thereon.

A planar substrate 20 having first side 16 and opposing side 18 is formed, and at least three through-slots 30 are formed in the substrate wherein each through-slot has a length 60 and width 62 sufficient to expose the rows of bond pads 22 of a die 12 or 14 bonded to the substrate to overlie the through-slot. The through-slot may be of uniform width 62, or may include a stepped surface(s) 58.

Conductive patterns 34A, 34B are formed on sides 16,18, respectively, of the substrate 20, such as by a lithographic metallization process or by other methods known in the art. The conductive patterns 34A, 34B include conductors 35 having one end configured as a wire-connecting site 32 adjacent a through-slot 30, and the other end is configured for attachment to an input/output connection. Where the through-slot 30 is stepped, the wire-connecting sites 32 are positioned on the stepped surfaces 58.

The formation of the through-slots 30 and the conductive patterns 34 may be in any order.

An input/output connection means is added to the module 10, and may comprise an array of solder balls 50 or pins, or may be a socket type edge connector 54.

Dice 12, 14 are then mounted on both sides 16, 18 of the substrate 20 with an adhesive layer 38. Each die is mounted so that all of its bond pads 22 to be connected are

positioned within a through-slot 30 and are thus exposed on the opposite side of the substrate 20 between two other dice, for wire-bonding.

Bond pads 22 of each die 12, 14 are wire-bonded by conductive wires 44 to the connecting sites 32 of the conductor patterns.

Typically, each die 12, 14 and/or all dice collectively are tested for operability before the through-slots 30 are filled with glob-top 40 to encapsulate and seal the wires 44 therein and spaces between adjacent dice 12, 14.

Optionally, the module, including the otherwise exposed die surfaces and substrate, may be encapsulated with a polymeric material.

The module 10 as described has a high density. The effective density increases as the number of dice 12, 14 is increased. Both sides of the substrate 20 are utilized, and the modules 10 so formed may be surface bonded to both sides of a printed circuit board (PCB) for example. Furthermore, the method may be used as chip-on-board (COB) technology for attaching a plurality of bare dice 12, 14 to a mother board without prior encapsulation.

The wire protection provided by the through-slots 30 and dice 12, 14 enables the module 10 to be electrically tested prior to glob-top encapsulation, without endangering the wires 44. This also enables easy and rapid removal and replacement of any defective die.

The method requires minimal glob-topping.

Additional advantages and modifications will readily be recognized by those skilled in the art. Therefore, the invention in its broader aspects is not limited to the specific details, and representative devices, shown and described herein, but includes various modifications which may be made without departing from the spirit or scope of the general inventive concept and embodiments as defined by the appended claims and their equivalents.

CLAIMS

What is claimed is:

1. A multi-chip module, comprising:

a substrate having a first side and a second side and at least two elongate through-slots extending from the first side to the second side thereof, said through-slots having a length and width;

electrical conductors formed on said first side and second side of said substrate, said electrical conductors having connection terminals adjacent said at least two through-slots for bonding portions of wires to bond pads exposed through said at least two through-slots;

electrical input/output connectors for connecting said electrical conductors to an external circuit;

a first semiconductor die having an active surface with a plurality of bond pads thereon, and a reverse surface, a portion of said active surface bonded to said first side of said substrate, at least one of the plurality of conductive bond pads on the active surface of the semiconductor die exposed through a through-slot in said substrate for bonding a portion of a wire to at least one conductor on said second side of said substrate;

a second semiconductor die having an active surface with a plurality of bond pads thereon, and a reverse surface, a portion of said active surface bonded to said first side of said substrate, at least one bond pad of the plurality of bond pads thereon exposed through a through-slot in said substrate for wire-bonding to at least one conductor on said first side of said substrate; and

at least two conductive wires connecting at least two of said bond pads on said first semiconductor die and said second semiconductor die to at least two of said connection terminals, one of said at least two connection terminals located on the first side of said substrate and the other of said at least two connection terminals located on the second side of said substrate, said first semiconductor die and said

second semiconductor die positioned wherein a conductive wire connected thereto extends through a through-slot in said substrate.

2. The multi-chip module of claim 1, further comprising glob-top sealant filling said at least two through-slots in said substrate.

3. The multi-chip module of claim 1, further comprising a layer of polymeric sealant encapsulating a portion of said module.

4. The multi-chip module of claim 1, wherein said first semiconductor die and said second semiconductor die are attached to said substrate at two different planes.

5. The multi-chip module of claim 1, wherein said electrical conductors on said first side of said substrate have connection terminals adjacent one through-slot in said substrate for wire-bonding to bond pads on said first semiconductor die attached to said second side, and said electrical conductors on said second side of said substrate have connection terminals adjacent another through-slot for wire-bonding to bond pads on said second semiconductor die attached to said first side of said substrate.

6. The multi-chip module of claim 1, wherein said electrical conductors comprise metallization patterns on said first and second sides of said substrate.

7. The multi-chip module of claim 1, further comprising:
conductive vias through said substrate and connecting electrical conductors on the first side and the second side of said substrate.

8. The multi-chip module of claim 1, wherein said electrical connectors comprise a ball-grid-array of solder balls on one side of said substrate.

9. The multi-chip module of claim 1, wherein said electrical connectors comprise an edge connector.

10. The multi-chip module of claim 1, wherein said electrical connectors comprise a socket connector.

11. A multi-chip module, comprising:

a substrate having a first side, a second side, and a plurality of elongate through-slots extending from the first side to the second side thereof, said through-slots having a length and width;

electrical conductors formed on said first side and second side of said substrate and having connection terminals adjacent said through-slots for wire-bonding to bond pads exposed through said through-slots;

electrical input/output connectors for connecting said electrical conductors to an external circuit;

a plurality of semiconductor dice, each semiconductor die of said plurality of semiconductor dice having an active surface having a plurality of bond pads thereon and a reverse surface, a plurality of said active surface bonded to said first side of said substrate, the bond pads of each semiconductor die exposed through a through-slot of said plurality of through-slots to said second side of said substrate for wire-bonding to conductors on said second side, at least one semiconductor die of said plurality of semiconductor dice attached to said second side of said substrate, the bond pads of said at least one semiconductor die of said plurality of semiconductor dice exposed through a through-slot to said first side of said substrate for wire-bonding to conductors on said first side of said substrate; and

conductive wires connecting said bond pads of said plurality of said semiconductor dice to said connection terminals, each said semiconductor die of said plurality of semiconductor dice positioned having conductive wires connected thereto extend

through a through-slot in a space between adjacent spaced dice on the opposite side of said substrate thereto.

12. The multi-chip module of claim 11, further comprising glob-top sealant covering said bond pads and conductive wires within said through-slots.

13. The multi-chip module of claim 12, wherein said glob-top sealant fills said space between adjacent semiconductor die.

14. The multi-chip module of claim 11, further comprising a layer of polymeric sealant encapsulating said module.

15. The multi-chip module of claim 11, wherein said dice are attached in a bi-planar configuration on said substrate.

16. The multi-chip module of claim 11, wherein said electrical conductors on said first side of said substrate have connection terminals adjacent alternate through-slots for wire-bonding to bond pads on semiconductor die of said plurality of semiconductor dice attached to said second side of said substrate, and said electrical conductors on said second side have connection terminals adjacent other through-slots for wire-bonding to bond pads on semiconductor die of said plurality of semiconductor dice attached to said first side.

17. The multi-chip module of claim 11, wherein said electrical conductors comprise metallization patterns on said first side and second side of said substrate.

18. The multi-chip module of claim 11, further comprising conductive vias through said substrate and connecting electrical conductors on opposite sides of said substrate.

19. The multi-chip module of claim 11, wherein said electrical connection means comprises a ball-grid-array of solder balls on one side of said substrate, in the periphery thereof about said attached dice.

20. The multi-chip module of claim 11, wherein said electrical connectors comprise an edge connector.

21. The multi-chip module of claim 11, wherein said electrical connectors comprise a socket connector.

22. The multi-chip module of claim 11, wherein the number of said plurality of semiconductor dice mounted on said second side of said substrate differs by one from the number of said plurality of semiconductor dice mounted on said first side of said substrate.

23. The multi-chip module of claim 11, wherein the length of said through-slot exceeds the length of said bond pads on a semiconductor die of said plurality of semiconductor dice.

24. The multi-chip module of claim 11, wherein said through-slot has uniform dimensions between said first side and said second side of said substrate.

25. The multi-chip module of claim 11, wherein the width of a through-slot of said plurality of through-slots is greater at one of said first and second sides of said substrate.

26. The multi-chip module of claim 25, wherein the width of a through-slot of said plurality of through-slots is configured to provide a step intermediate said first side and said second side of said substrate.

27. The multi-chip module of claim 26, wherein said connection terminals of the electrical conductors are positioned on said step.

28. The multi-chip module of claim 25, wherein said through-slot is beveled between said first side and second side of said substrate.

29. The multi-chip module of claim 11, wherein said bond pads of a semiconductor die of said plurality of semiconductor dice are positioned along a center line of said active surface.

30. The multi-chip module of claim 11, wherein at least two semiconductor die of said plurality of semiconductor dice attached to said first side of said substrate lie in a first plane and at least two semiconductor die of said plurality of semiconductor dice attached to said second side of said substrate lie in a second plane.

31. The multi-chip module of claim 11, wherein said module comprises a memory device wherein a majority of said plurality of semiconductor dice have internal circuits.

32. A method for forming a high density multi-chip module, comprising the steps of:

providing a plurality of integrated circuit semiconductor dice, each semiconductor die having an active surface having a plurality of bond pads thereon;

forming a substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side, each said through-slot configured for opposite side access between attached semiconductor die of said plurality of semiconductor dice to the bond pads of a semiconductor die of said plurality of semiconductor dice bonded to said substrate;

forming a pattern of a plurality of electrical conductors associated with said substrate, at least one electrical conductor of said plurality of electrical conductors having a

connection terminal adjacent a through-slot of said at least three through-slots for connecting said bond pads of a semiconductor die of said plurality of semiconductor dice to an input/output connector;

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors;

attaching the active surfaces of a plurality of said semiconductor dice to a first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots for access from the second side of said substrate;

attaching the active surface of at least one semiconductor die of said plurality of semiconductor dice to said second side of said substrate, the bond pads of said at least one semiconductor die aligned with other alternate through-slots for access from the first side of said substrate; and

wire-bonding said bond pads of each attached semiconductor die of said plurality of semiconductor dice to connection terminals adjacent the corresponding through-slot.

33. The method of claim 32, wherein the step of forming through-slots comprises forming an elongate stepped surface in said through-slot.

34. The method of claim 33, wherein the step of forming a pattern of electrical conductors includes forming conductive connection terminals on said stepped surface.

35. The method of claim 32, further comprising the step of:

inserting a flowable hardenable glob-top material into each said through-slot to encapsulate the wires therein.

36. The method of claim 35, wherein a hardenable polymeric material is inserted into said through-slot.

37. The method of claim 35, wherein said glob-top material is inserted to extend outwardly between the edges of at least two semiconductor die of said plurality of semiconductor dice proximate each side of said through-slot.

38. The method of claim 32, further comprising the step of:
performing electrical testing of said plurality of semiconductor dice following wire-bonding thereof and prior to wire encapsulation.

39. The method of claim 32, comprising the further step of:
encapsulating said dice with a polymeric sealant.

40. The method of claim 32, wherein the step of forming a pattern of electrical conductors on said substrate comprises forming a conductor pattern on each of said first side and second side of said substrate.

41. The method of claim 40, further comprising the step of:
connecting said two conductor patterns with conductive vias through said substrate.

42. The method of claim 41, wherein the step of forming an input/output connector comprises forming one of a ball-grid-array and a pin-grid-array on one of said sides in a peripheral area surrounding said plurality of semiconductor dice.

43. The method of claim 42, wherein the step of forming an input/output connector comprises forming a socket connector on an edge of said substrate.

44. A method for forming a high density multi-chip module, comprising the steps of:
providing a plurality of integrated circuit dice, each die having an active surface with a row of conductive bond pads;

forming a planar substrate with opposing first and second sides, at least three elongate through-slots extending from said first side to said second side, each said through-slot configured for opposite side access between attached dies to the conductive bond pads of a die bonded to said substrate;

forming a pattern of electrical conductors associated with said substrate and having connection terminals adjacent each said through-slot for connecting said bond pads to an input/output connection means;

forming an input/output connector on said substrate and connecting said input/output connector to said electrical conductors from said bond pads;

attaching the active surfaces of a plurality of said dice to a first side of said substrate wherein the bond pads thereof are aligned with alternate through-slots for access from the second side;

attaching the active surface of at least one of said dice to said second side of said substrate wherein the bond pads thereof are aligned with other alternate through-slots for access from the first side; and

wire-bonding said bond pads of each attached die to connection terminals adjacent the corresponding through-slot.

45. The method of claim 44, wherein the step of forming through-slots comprises forming an elongate stepped surface in said through-slot.

46. The method of claim 44, wherein the step of forming a pattern of electrical conductors includes forming conductive connection terminals on said stepped surface.

47. The method of claim 44, further comprising the step of inserting a flowable hardenable glob-top material into each said through-slot to encapsulate the wires therein.

48. The method of claim 47, wherein a hardenable polymeric material is inserted into said through-slot.

49. The method of claim 47, wherein said glob-top material is inserted to extend outwardly between the edges of dice proximate each side of said through-slot.

50. The method of claim 44, further comprising the step of:
performing electrical testing of said dice following wire-bonding thereof and prior to wire encapsulation.

51. The method of claim 44, comprising the further step of:
encapsulating said dice with a polymeric sealant.

52. The method of claim 44, wherein the step of forming a pattern of electrical conductors on said substrate comprises forming a conductor pattern on each of said first and second sides.

53. The method of claim 52, further comprising the step of:
connecting said two conductor patterns with conductive vias through said substrate.

54. The method of claim 44, wherein the step of forming an input/output connector comprises forming one of a ball-grid-array and a pin-grid-array on one of said sides in a peripheral area surrounding said dice.

55. The method of claim 44, wherein the step of forming an input/output connector comprises forming a socket connector on an edge of said substrate.

ABSTRACT OF THE DISCLOSURE

A high density multi-chip module and method for construction thereof, wherein a plurality of integrated circuit dice with at least one row of generally central bond pads are bonded in a staggered flip-chip style, to opposite sides of a metallized substrate. The bond pads of each die are positioned over a through-hole in the substrate, and the bond pads are wire-bonded from the opposite side to circuitry on the opposing side of the substrate. Application of glob-top sealant into the through-holes seals the bond pads and bond wires. A ball grid array may be formed in the peripheral area surrounding the dice on one side of the substrate, or an edge connector may be incorporated for connection to an external circuit.

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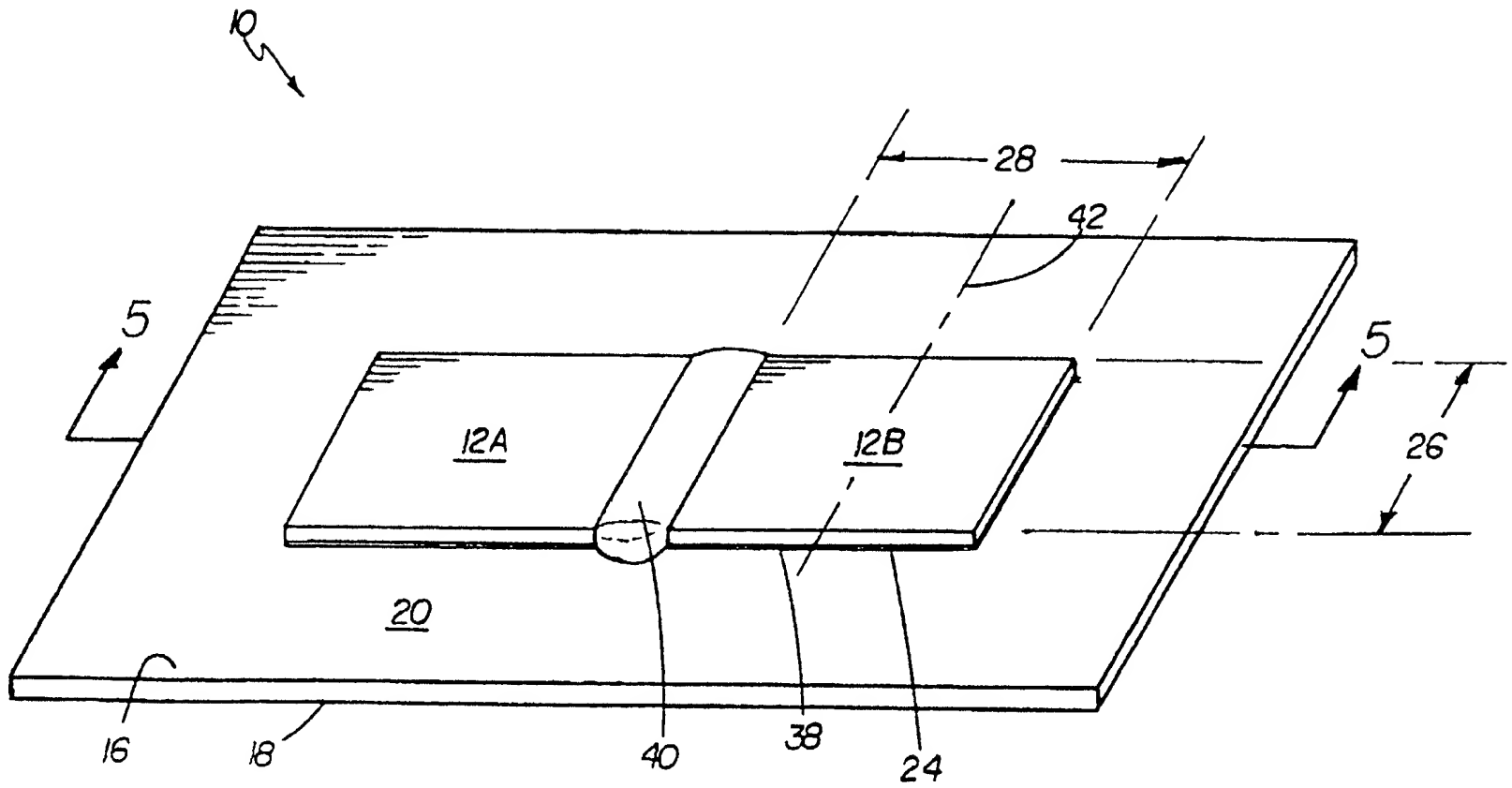


FIG. 1

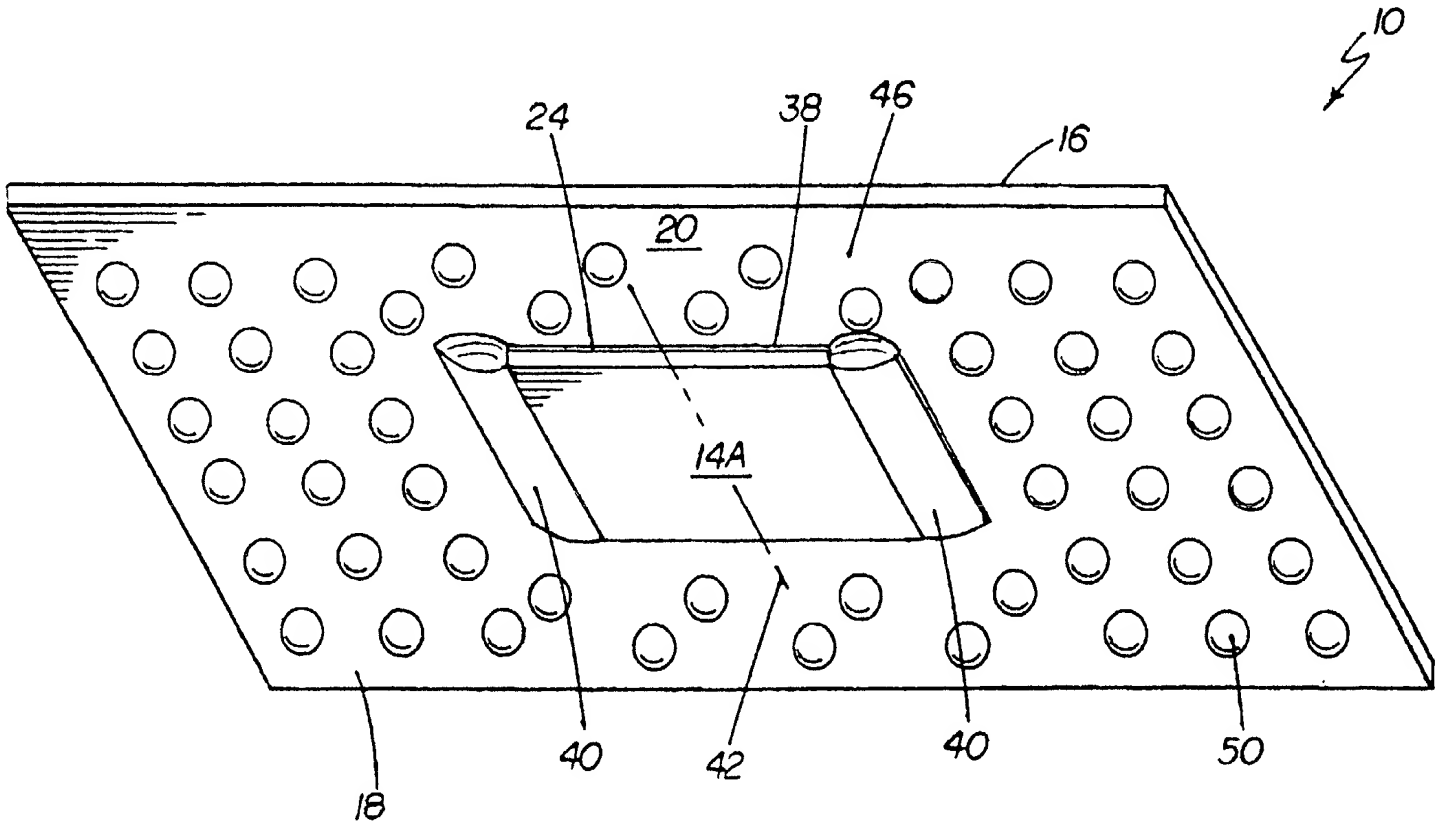
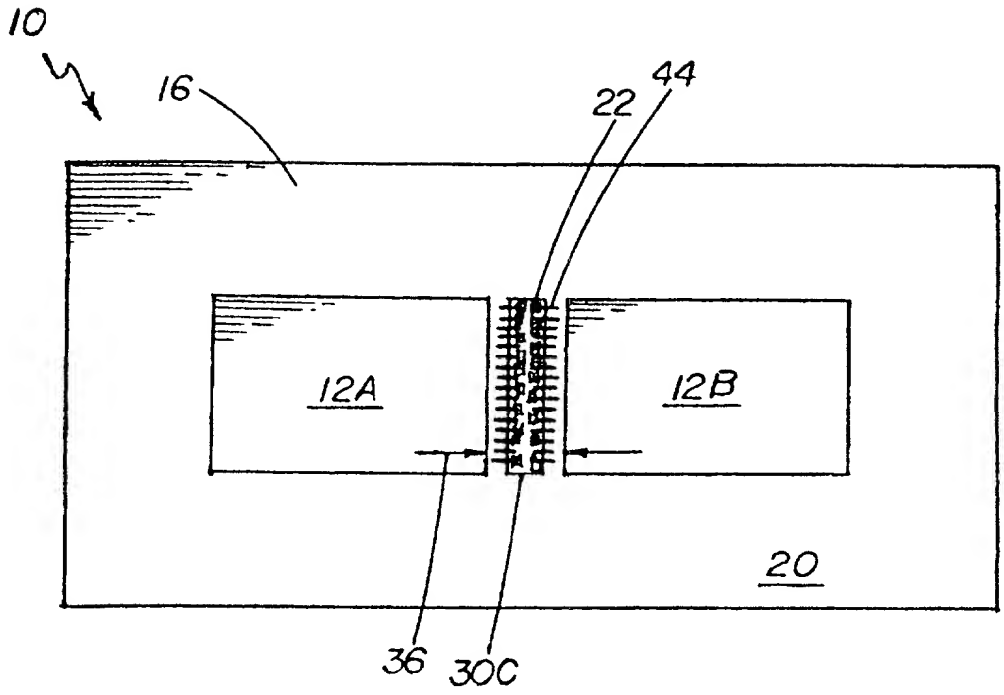


FIG. 2



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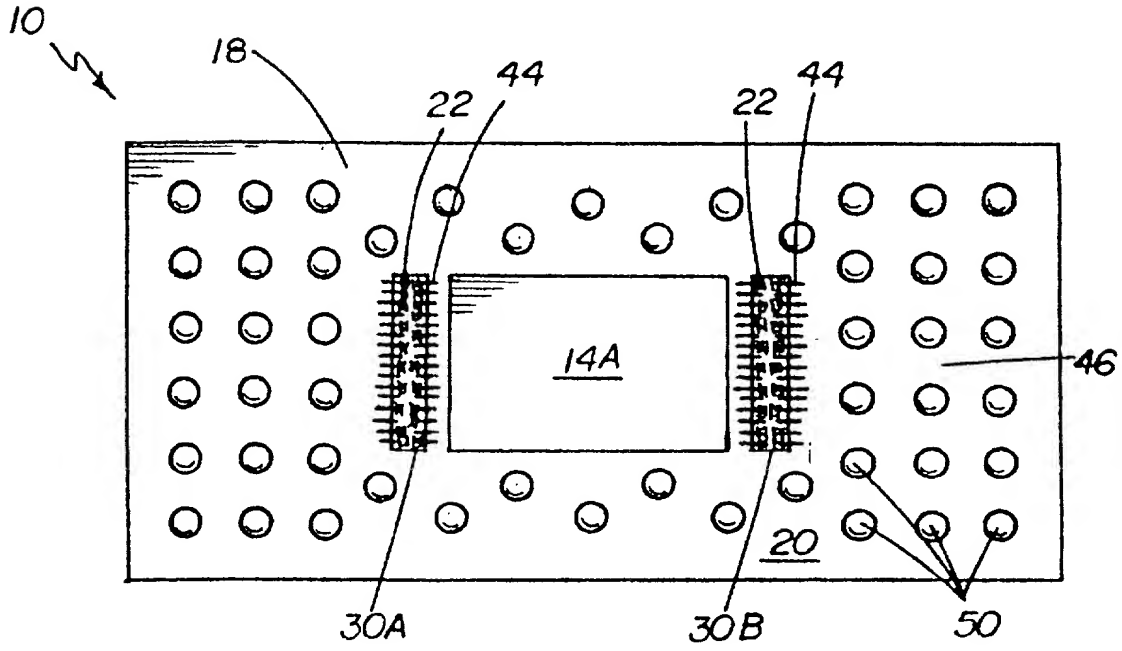
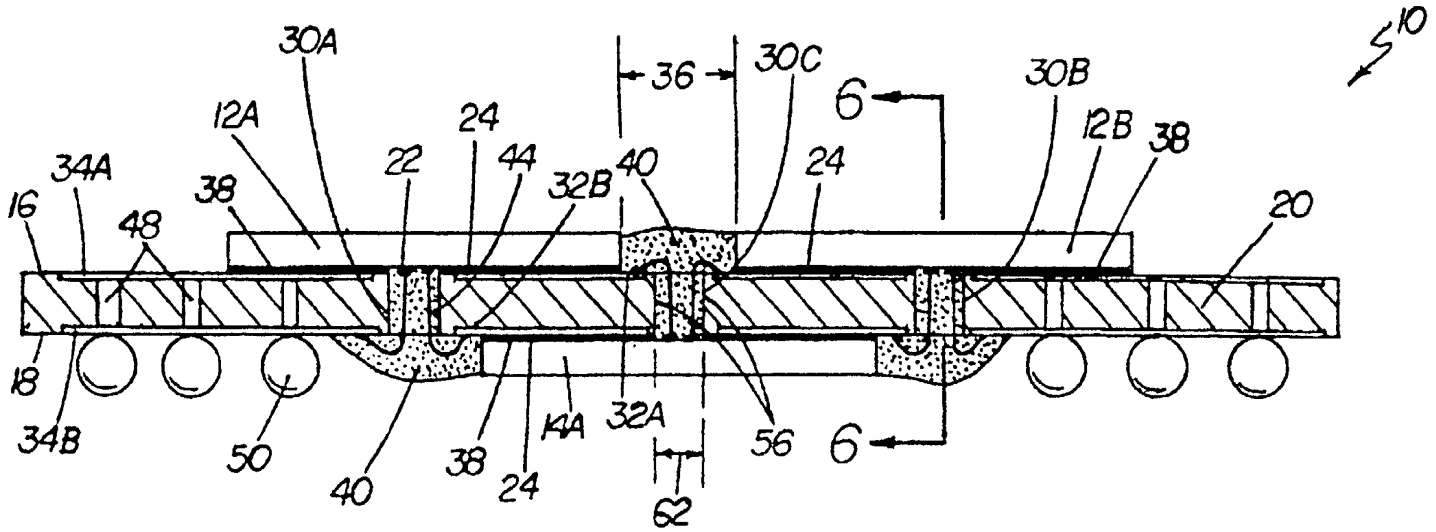


FIG. 4



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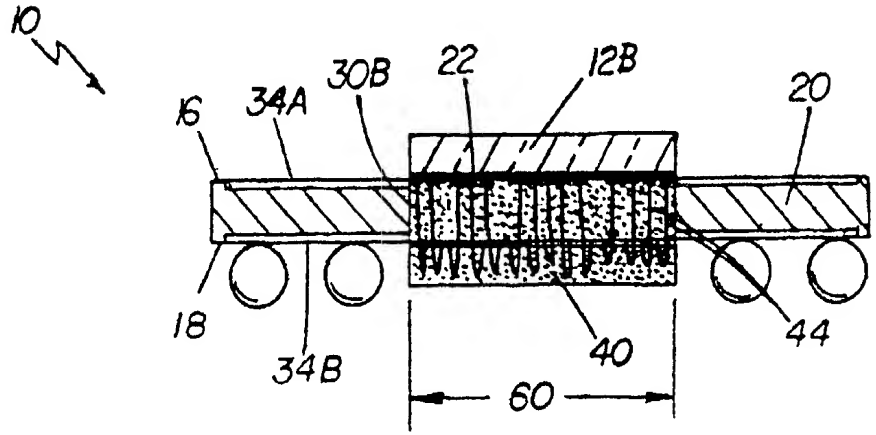

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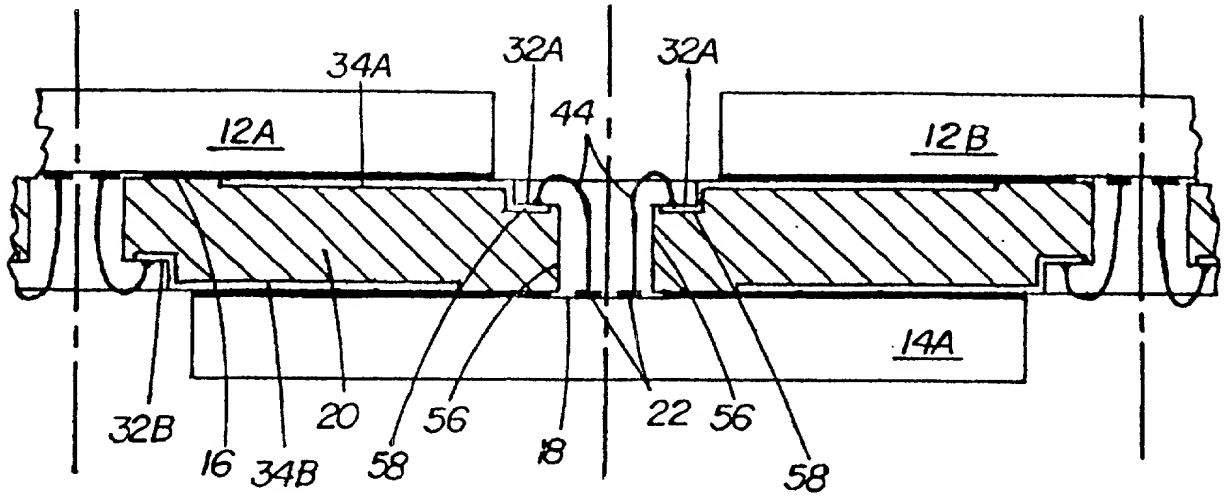
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32A
44
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12B
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32B
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34B
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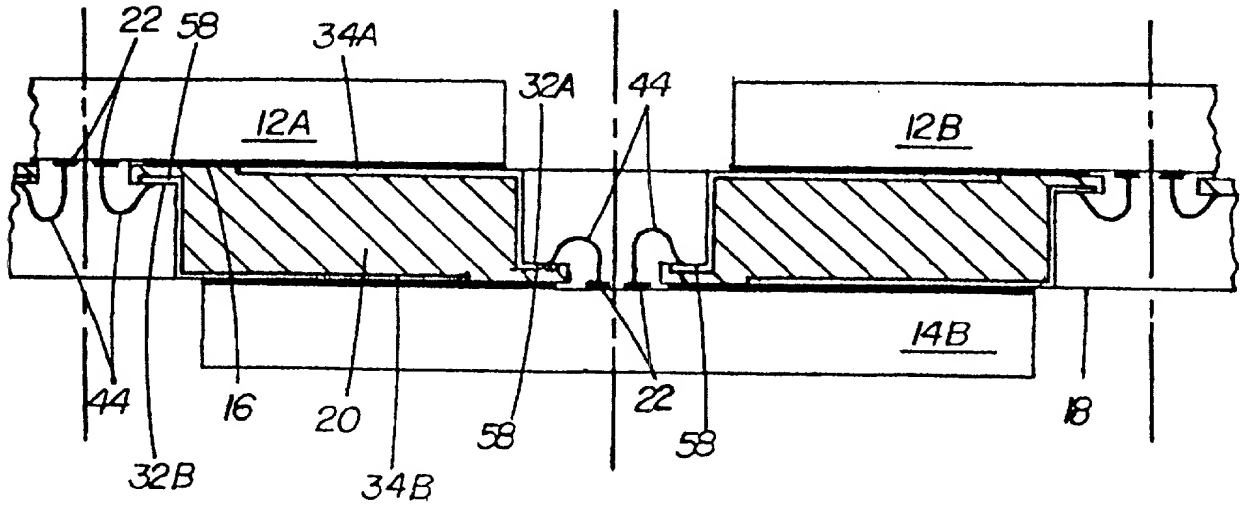
56
58
18
22
56
58

FIG. 7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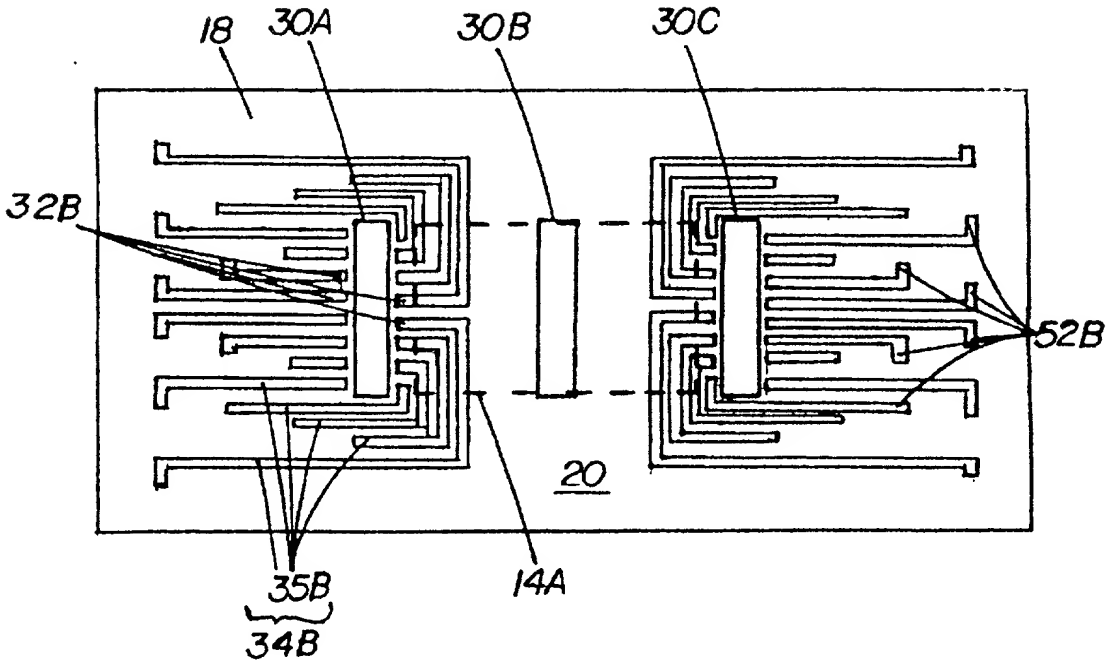
32B
34B

FIG. 8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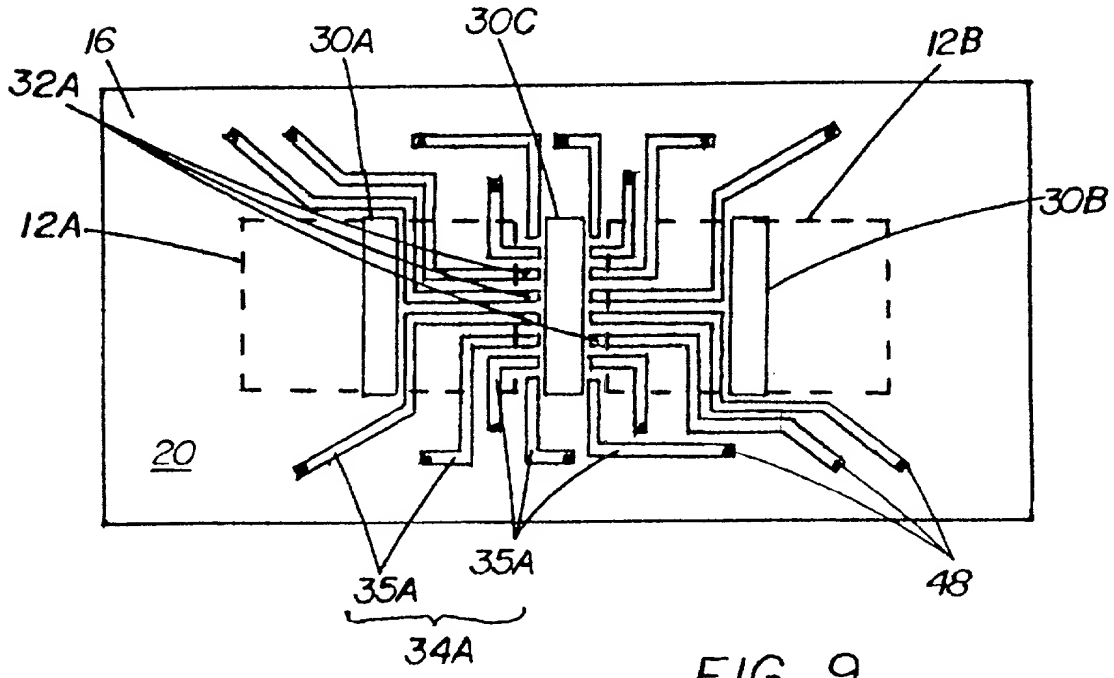
35B
34B
14A

FIG. 10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35A
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FIG. 9

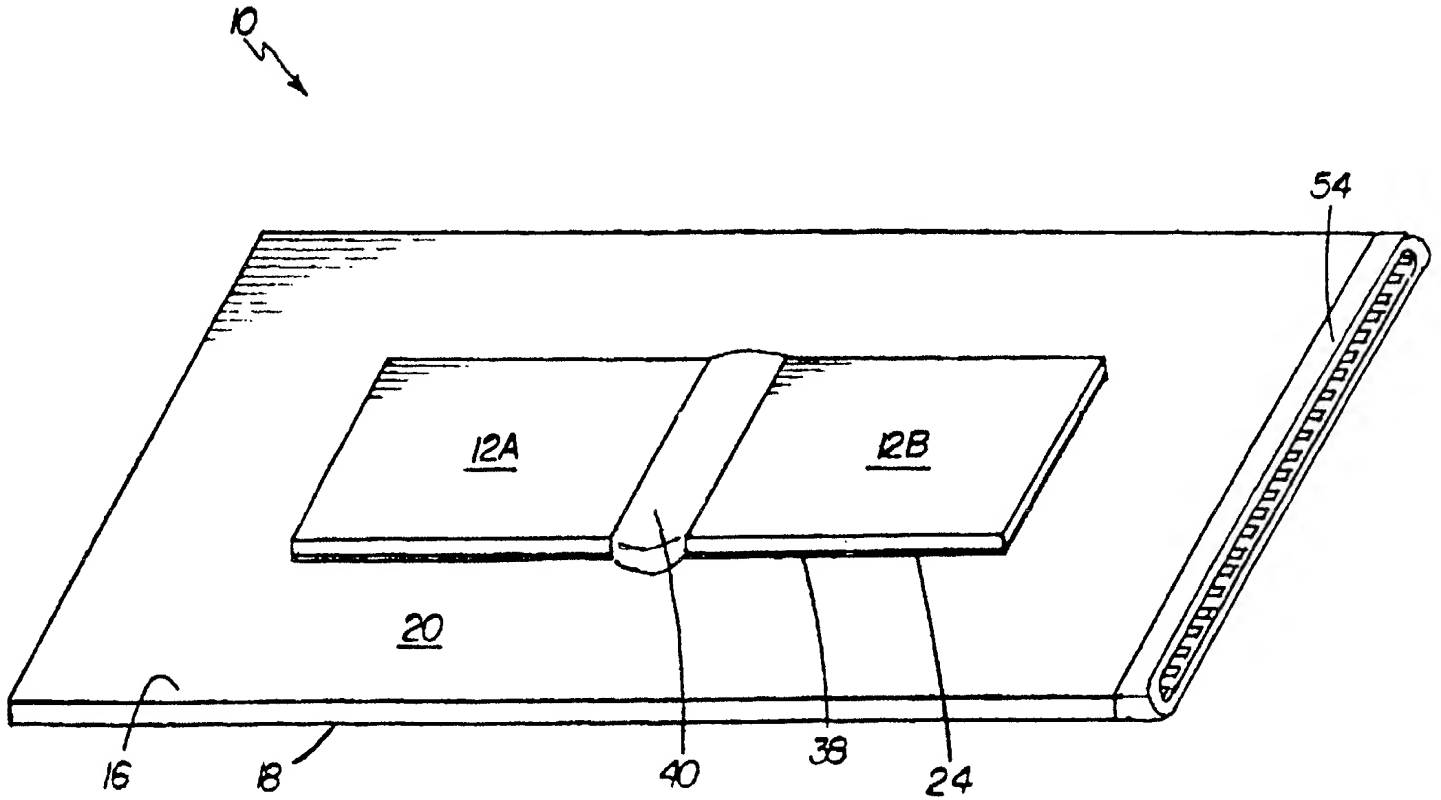
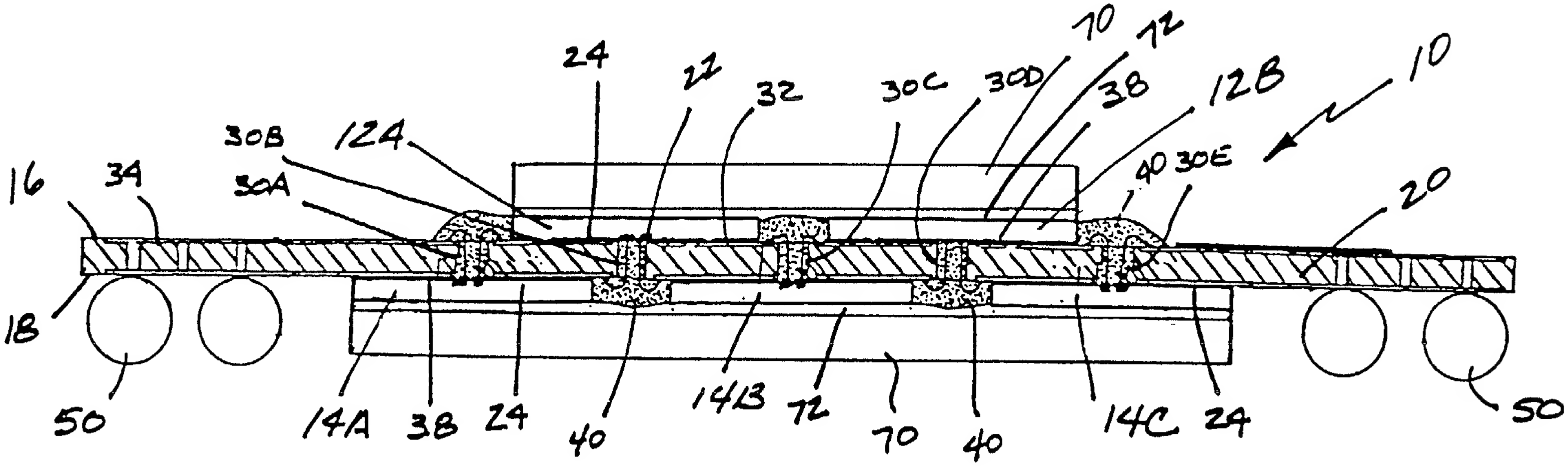


FIG. 11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72

FIG. 12

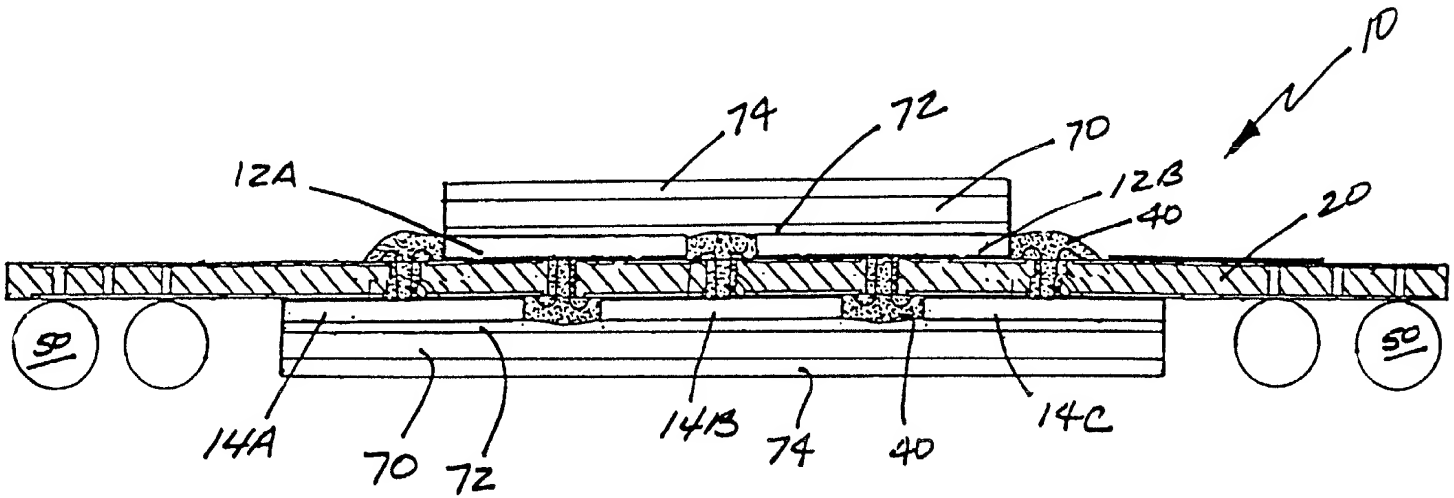

FIG. 13

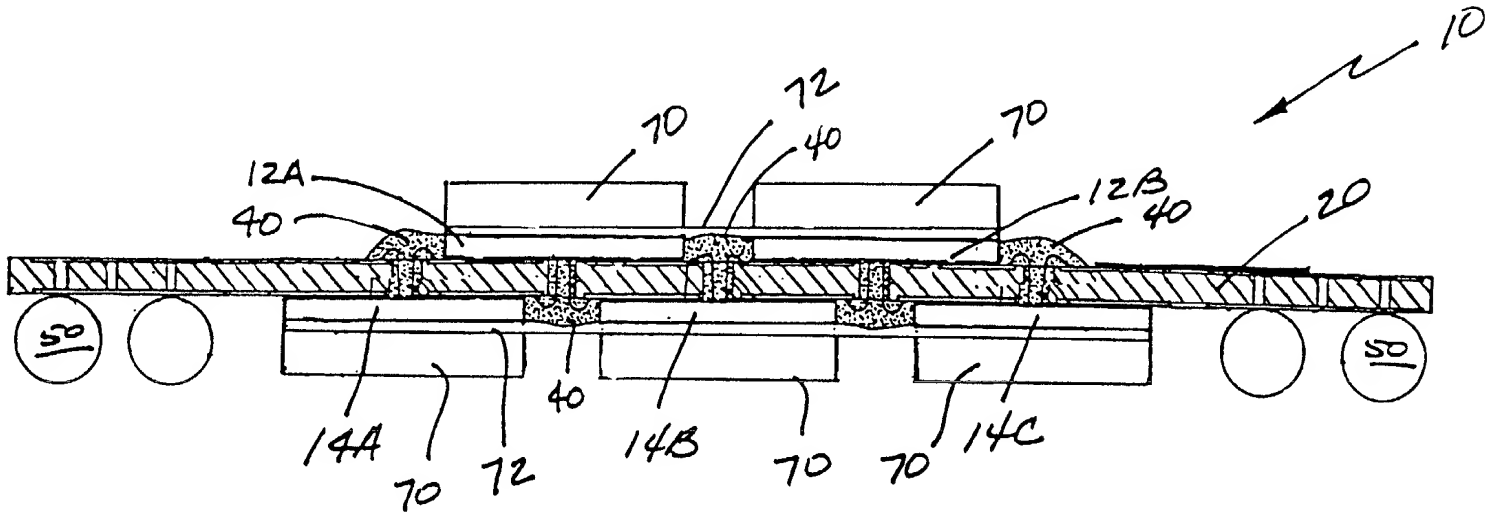

FIG. 14

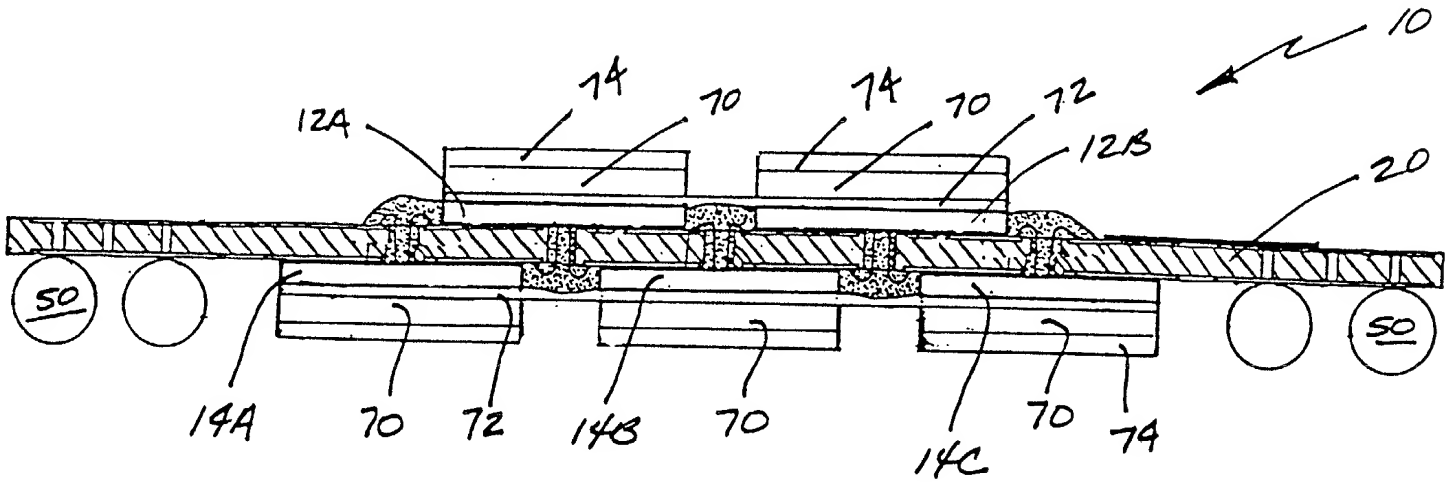

FIG. 15

DECLARATION FOR PATENT APPLICATION (WITH POWER OF ATTORNEY)

As an inventor named below or on any attached continuation page, I hereby declare that:

My residence, post office address and citizenship are as stated next to my name.

I believe that I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled **HIGH DENSITY MODULARITY FOR IC'S**, the specification of which (check one):

- ☒ is attached hereto.
- ☐ was filed on _____ as United States application serial no. _____ and was amended on _____.
- ☐ was filed on _____ as PCT international application no. _____ and was amended under PCT Article 19 on _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate or § 365(a) of any PCT international application(s) designating at least one country other than the United States of America listed below and on any attached continuation page and have also identified below and on any attached continuation page any foreign application for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America having a filing date before that of the application(s) on which priority is claimed.

Prior foreign/PCT application(s):

			Priority Claimed	
(number)	(country)	(day/month/year filed)	Yes	No
(number)	(country)	(day/month/year filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or § 365(c) of PCT international application(s) designating the United States of America listed below and on any attached continuation page and, insofar as the subject matter of each of the claims of this application is not disclosed in any such prior application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose to the U.S. Patent and Trademark Office all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations § 1.56 which became available between the filing date of such prior application and the national or PCT international filing date of this application.

(application serial no.)	(filing date)	(status - pending, patented or abandoned)
(application serial no.)	(filing date)	(status - pending, patented or abandoned)

I hereby claim the benefit under Title 35, United States Code, § 119(e) of any United States provisional application(s) listed below.

(provisional application no.)	(filing date)

I hereby appoint the following Registered Practitioners to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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Allen C. Turner, Reg. No. 33,041
Robert G. Winkle, Reg. No. 37,474
Kenneth C. Booth, Reg. No. 42,342
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Kent S. Burningham, Reg. No. 30,453
Edgar R. Cataxinos, Reg. No. 39,931
Samuel E. Webb, Reg No. P-44,394
Thomas J. Rossa, Reg. No 26,799
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Julie K. Morriss, Reg No. 33,263
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Michael L. Lynch, Reg No. 30,871

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TRASK, BRITT & ROSSA
P.O. BOX 2550
Salt Lake City, Utah 84110

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Inventor's signature Salman Akram Date 1/8/99 1/8/99
Salman Akram
Residence: Boise, ID
Citizenship: Pakistan
Post Office Address: 1463 E. Regatta, Boise, ID 83706

Full name of second joint inventor: Jerry M. Brooks
Inventor's signature Jerry M Brooks Date 1/11/99
Residence: Caldwell, ID
Citizenship: U.S.A.
Post Office Address: 1914 Ray Avenue, Caldwell, ID 83605

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant:	Salman Akram et al.	**Examiner:**	Unknown
Serial No.:	Not yet assigned	**Group Art Unit:**	Unknown
Filed:		**Attorney Docket No.:**	3638US (98-0093)
Title:	HIGH DENSITY MODULARITY FOR IC'S		

POWER OF ATTORNEY BY ASSIGNEE
AND CERTIFICATE UNDER 37 CFR § 3.73(b)

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

MICRON TECHNOLOGY, INC., assignee of the entire right, title and interest by assignment from the inventor(s) in the above-identified application, hereby appoints the following attorneys and agents:

David V. Trask, Reg. No. 22,012	William S. Britt, Reg. No. 20,969	Thomas J. Rossa, Reg. No. 26,799
Laurence B. Bond, Reg. No. 30,549	Joseph A. Walkowski, Reg. No. 28,765	James R. Duzan, Reg. No. 28,393
Allen C. Turner, Reg. No. 33,041	Kent S. Burningham, Reg. No. 30,453	Julie K. Morriss, Reg. No 33,263
Robert G. Winkle, Reg. No. 37,474	Edgar R. Cataxinos, Reg. No. 39,931	Brick G. Power, Reg. No 38,581
Kenneth C. Booth, Reg. No. 42,342	Samuel E. Webb, Reg. No. P-44,394	Michael L. Lynch, Reg. No. 30,871
Lia M. Pappas, Reg. No. 34,095		

as its attorneys with full power of substitution to prosecute this application and to transact all business in the U.S. Patent and Trademark Office in connection therewith.

The above-identified assignee hereby elects, pursuant to 37 C.F.R. § 3.71, to conduct the prosecution of the above-identified patent application to the exclusion of the inventor(s).

A chain of title from the inventor(s) of the above-identified patent application to the above-identified assignee is shown:

☐ In an assignment recorded in the U.S. Patent and Trademark Office at Reel , Frame .

☒ In an assignment filed herewith for recordation, a true copy of which is attached hereto.

The undersigned has reviewed the above-identified assignment and, to the best of his knowledge and belief, title is in the above-identified assignee.

The undersigned further avers that he is empowered to make and sign the foregoing certification on behalf of the above-identified assignee, and to take the action set forth herein on its behalf.

Please direct all communications regarding the above-identified application to:

James R. Duzan,
TRASK, BRITT & ROSSA
P.O. Box 2550
Salt Lake City, UT 84110
Tele: (801) 532-1922
Fax: (801) 531-9168

Respectfully Submitted,

MICRON TECHNOLOGY, INC

Date: Jan 13, 1999

By: _____
Michael L. Lynch, Esq.
Reg. No. 30,871
Chief Patent Counsel,
MICRON TECHNOLOGY, INC.

N:\2269\3638\Assent of Assignee.wpd 1/7/99